

FIG. 1

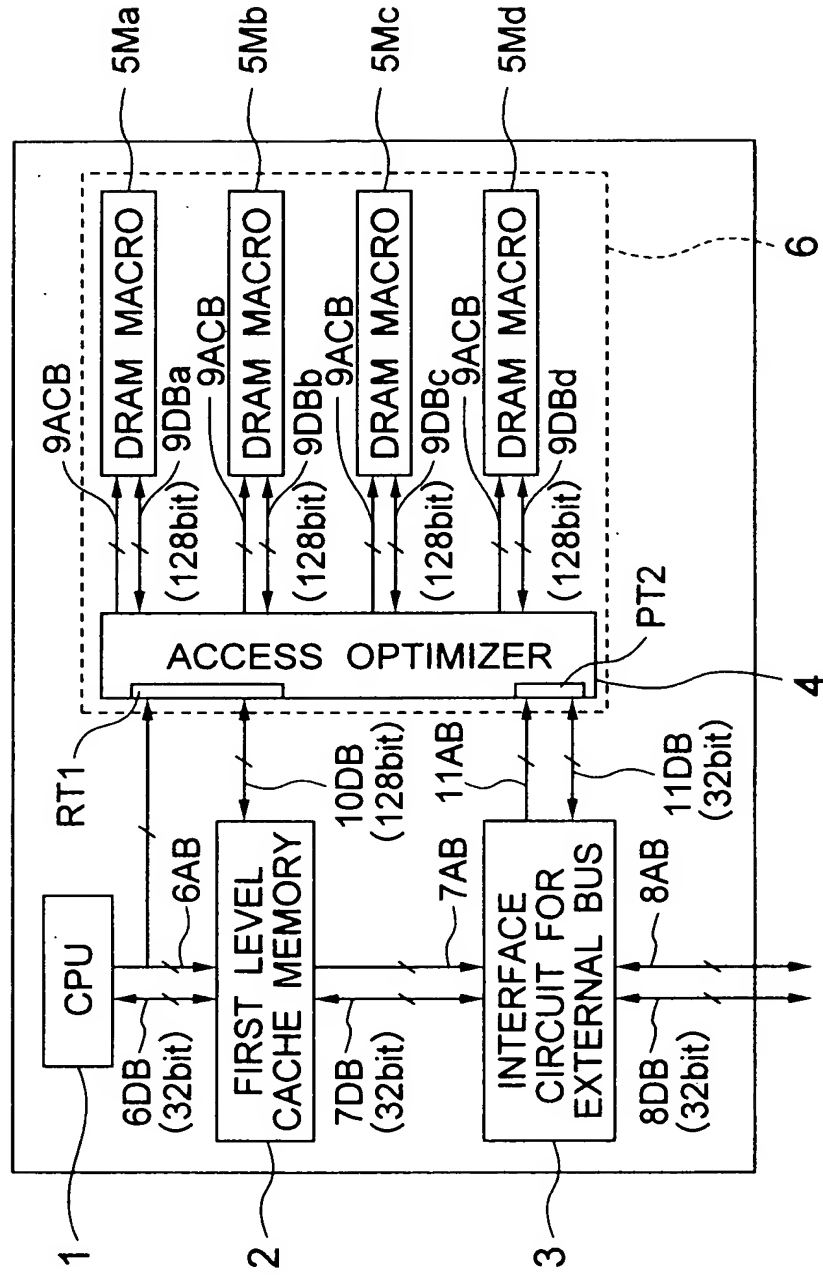


FIG. 2

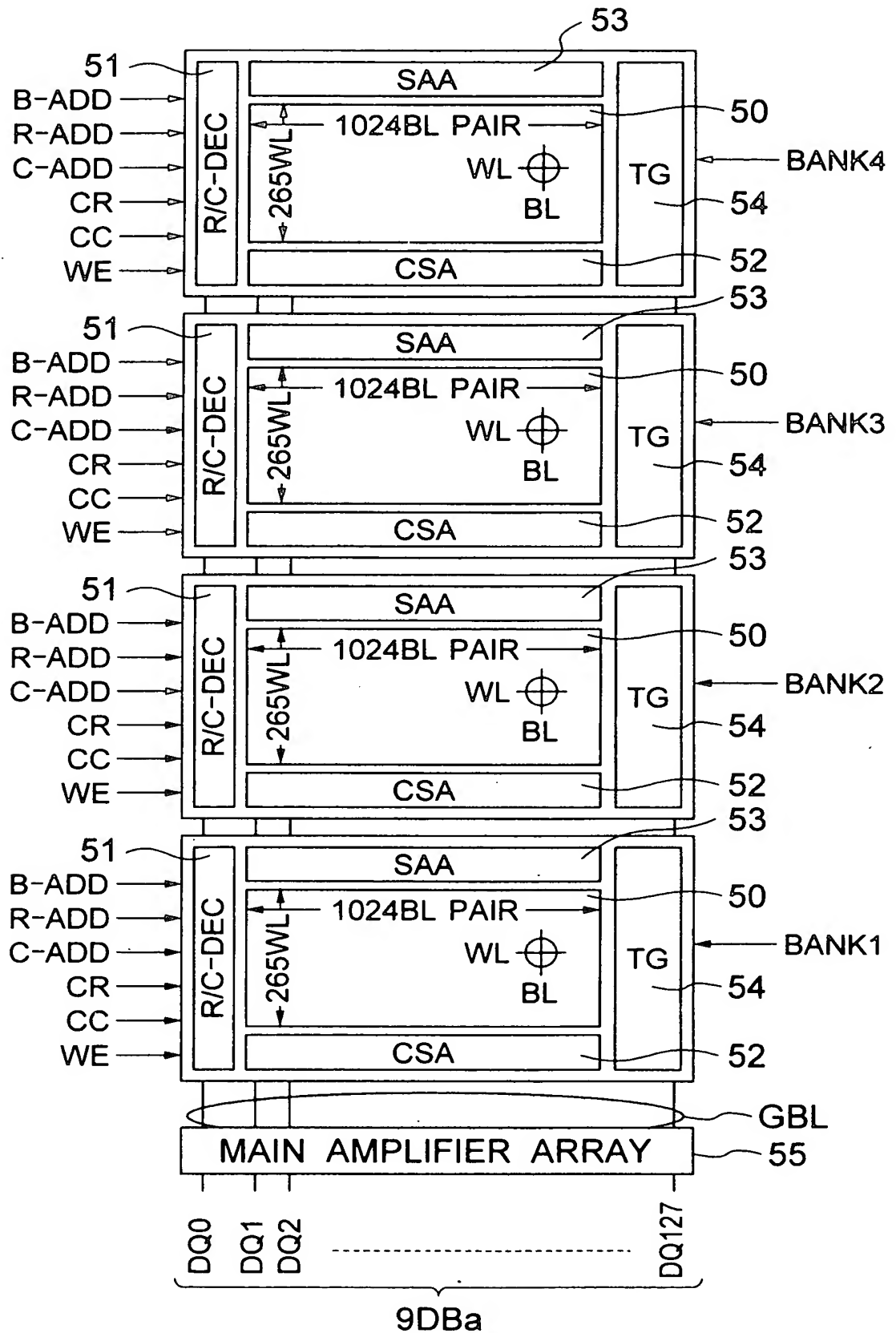


FIG. 3

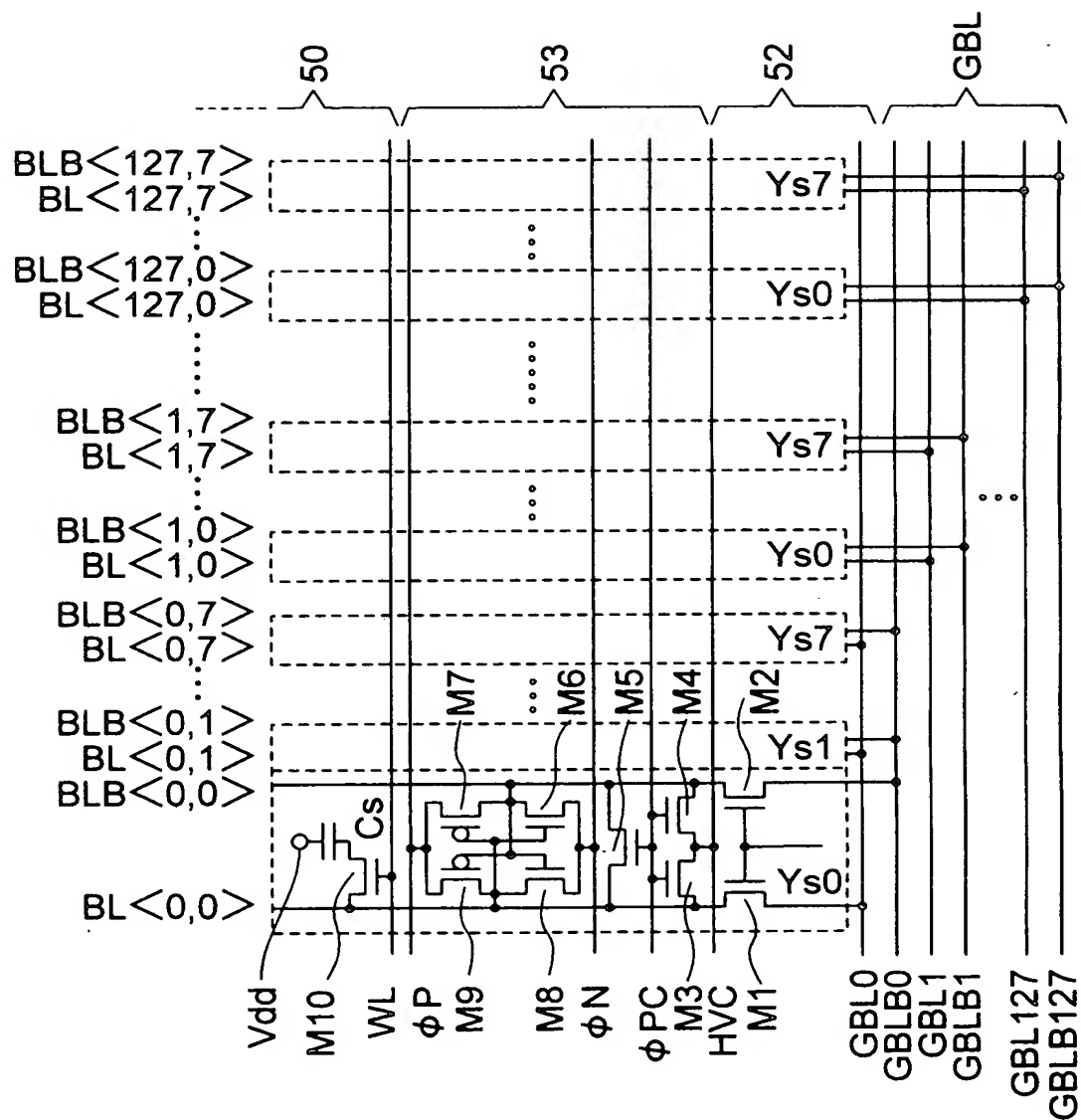


FIG. 4

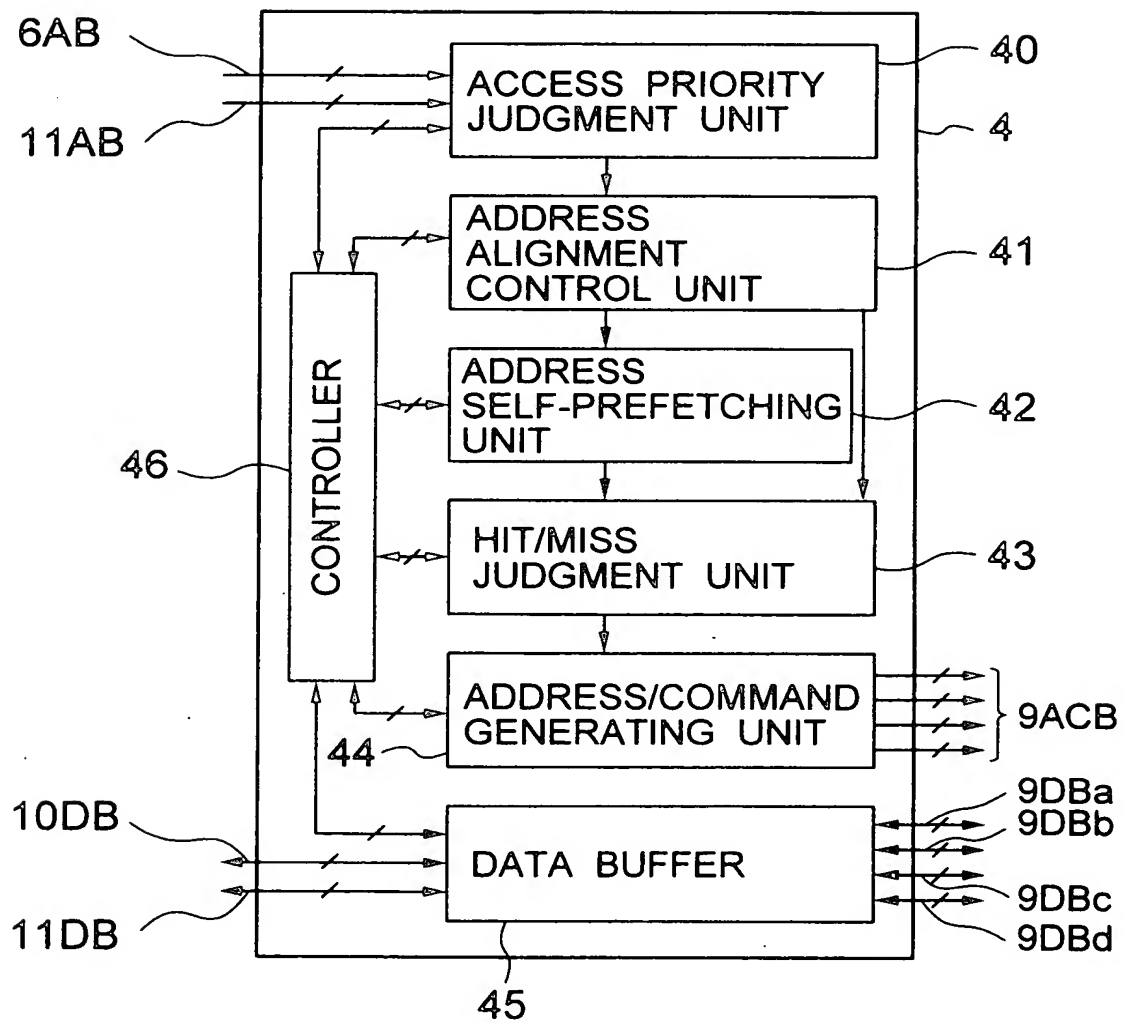


FIG. 5

L1-CACHE(4WAY)

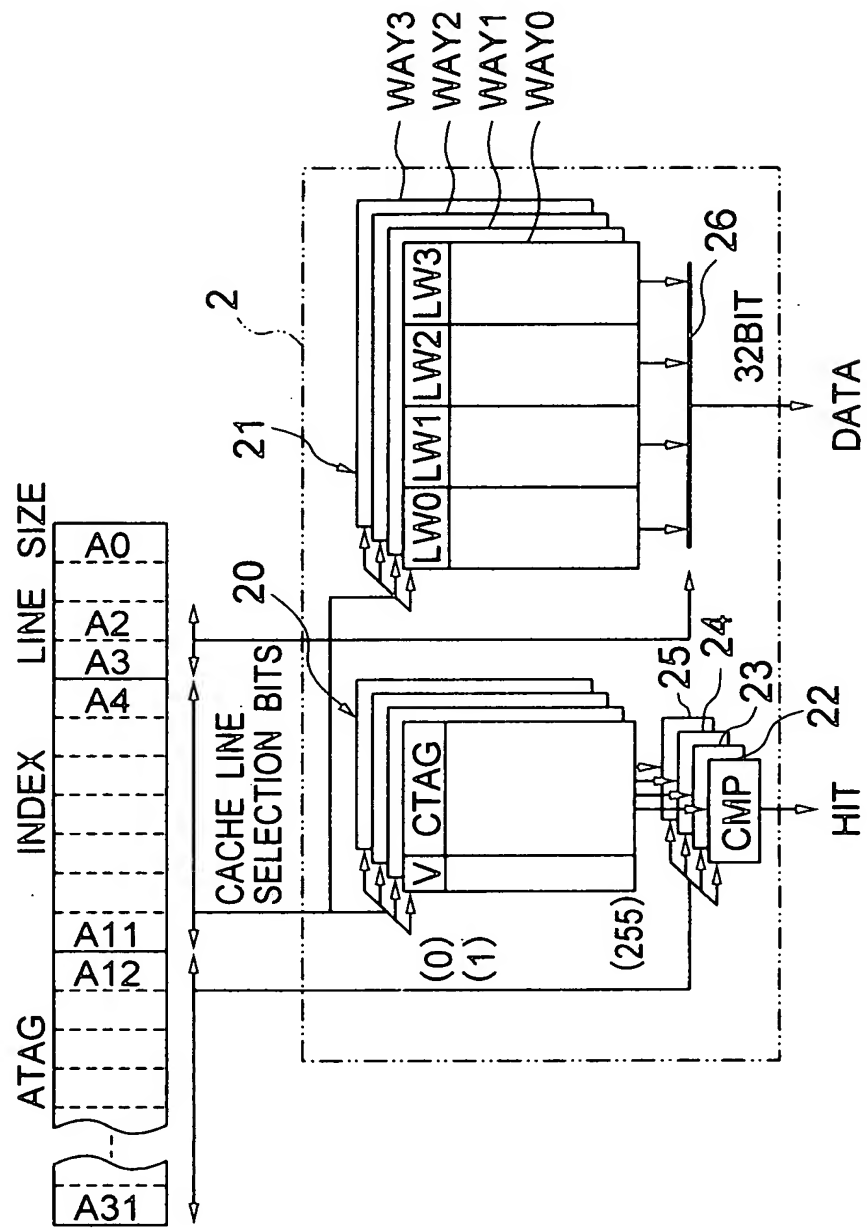


FIG. 6

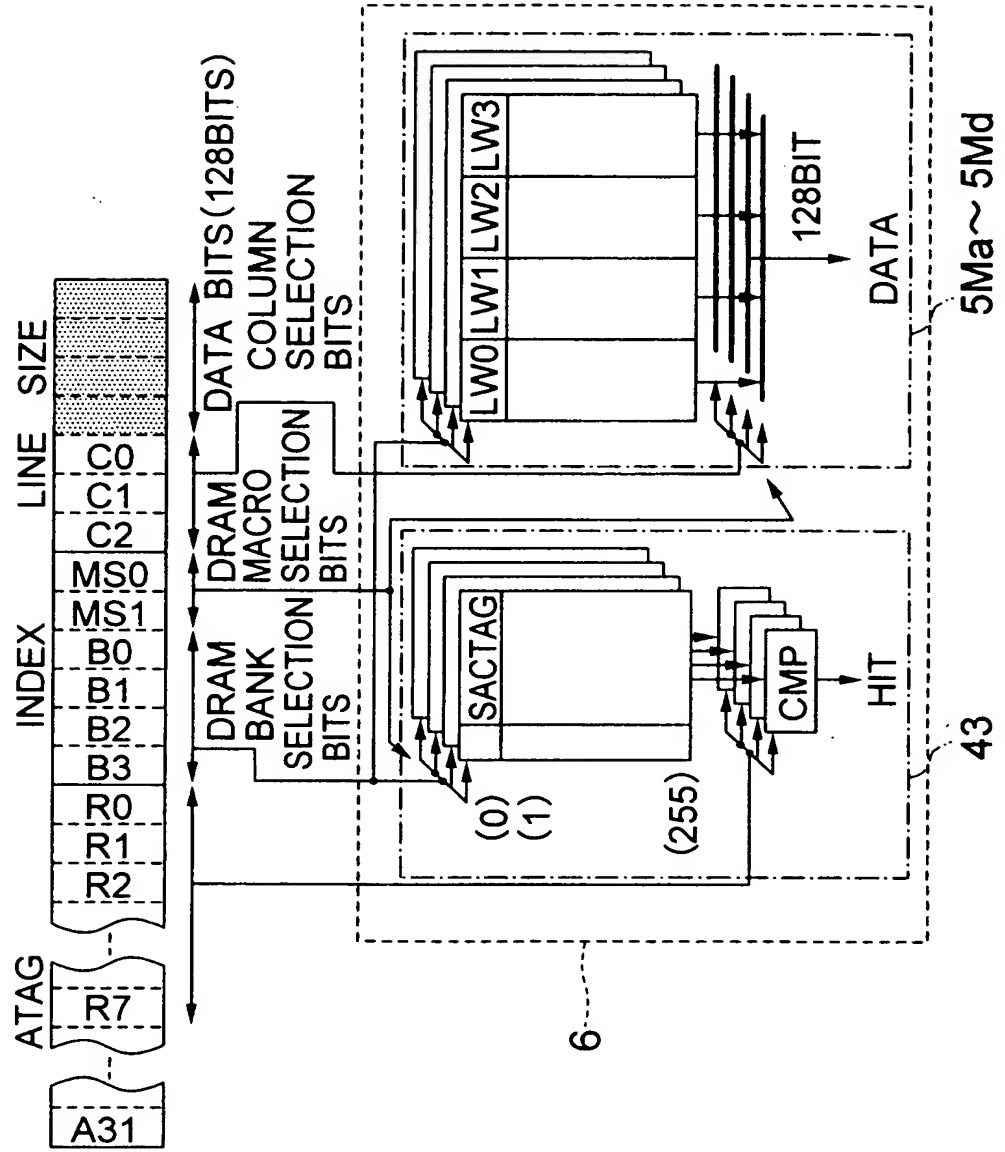


FIG. 7

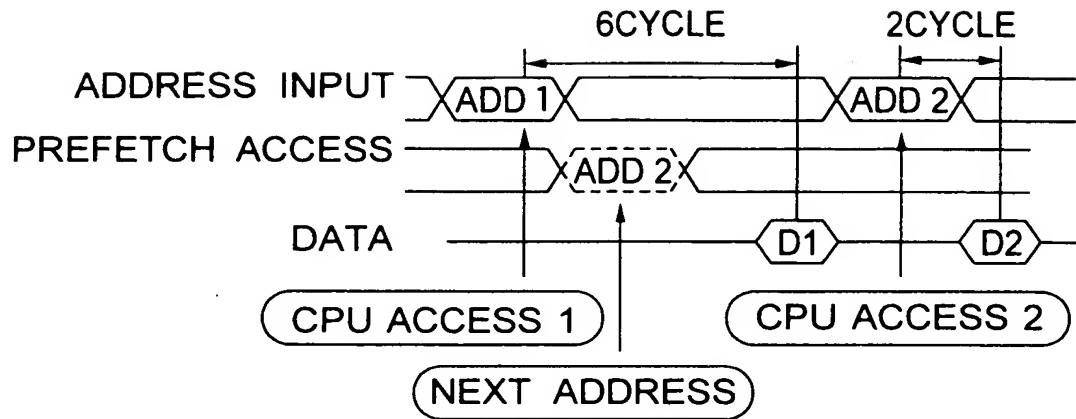


FIG. 8

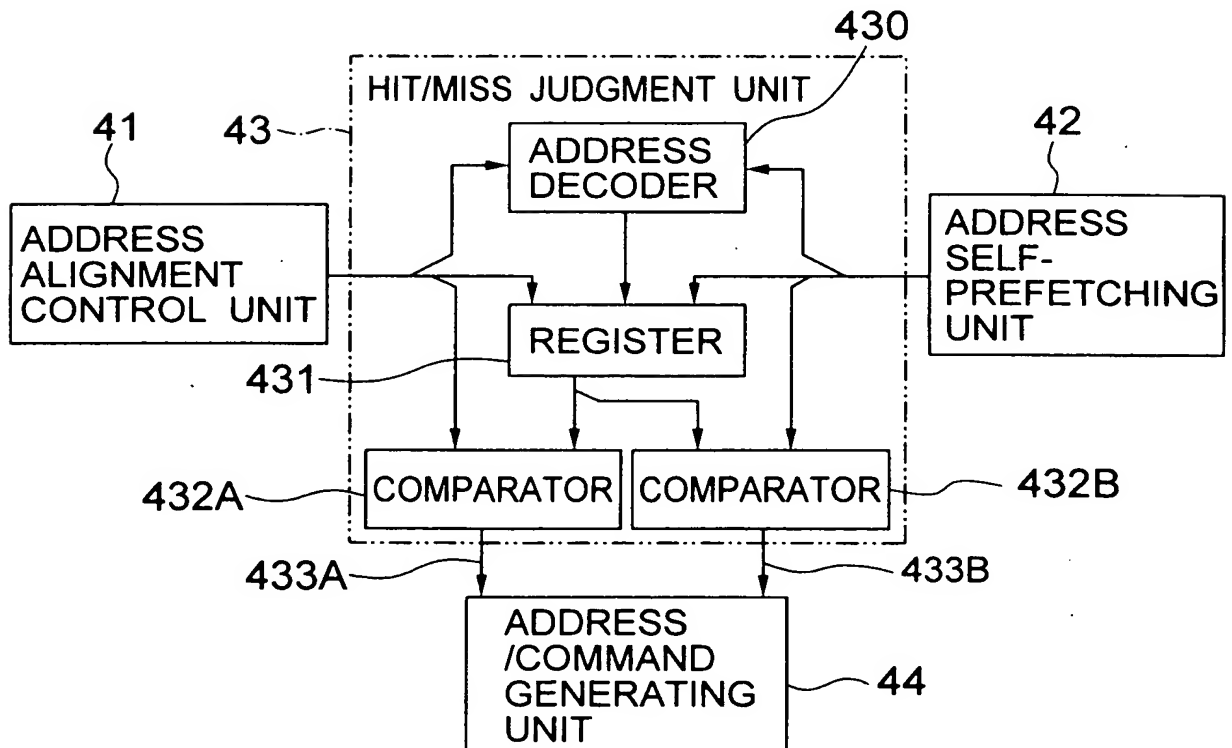


FIG. 9

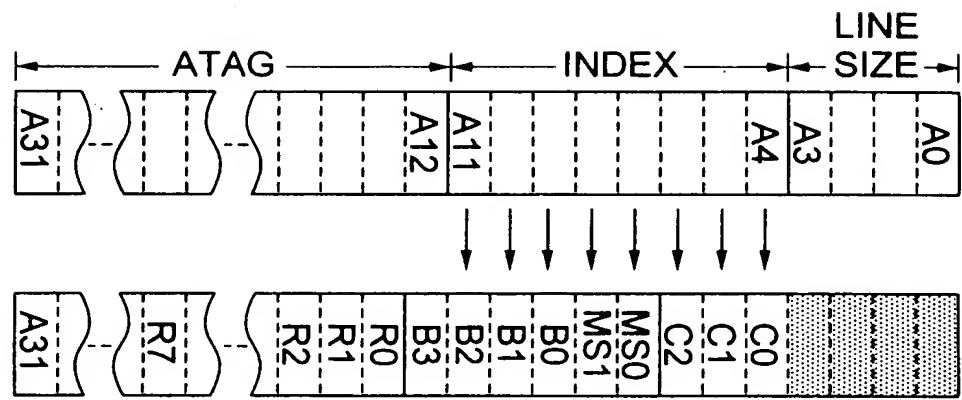


FIG. 10

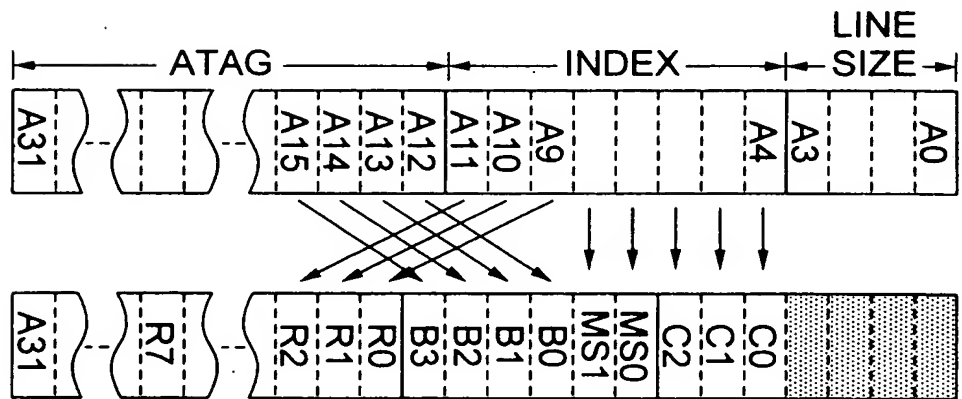


FIG. 11

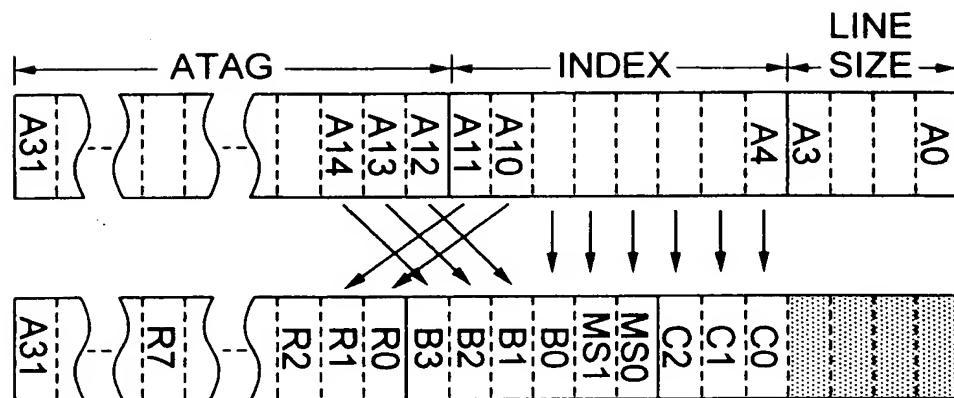


FIG. 12

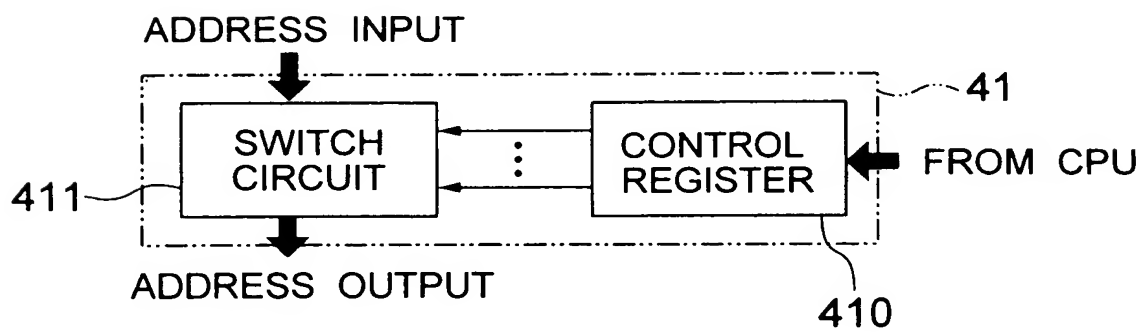


FIG. 13

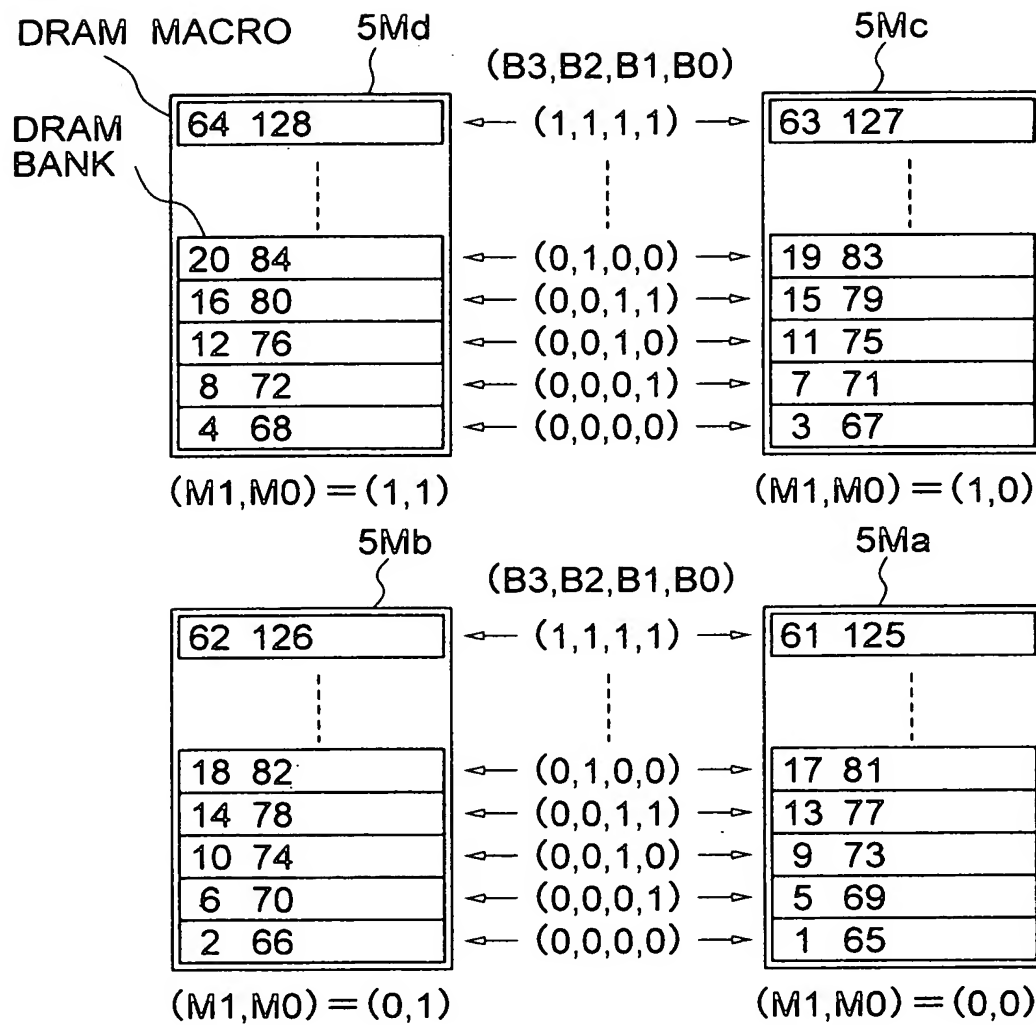


FIG. 14

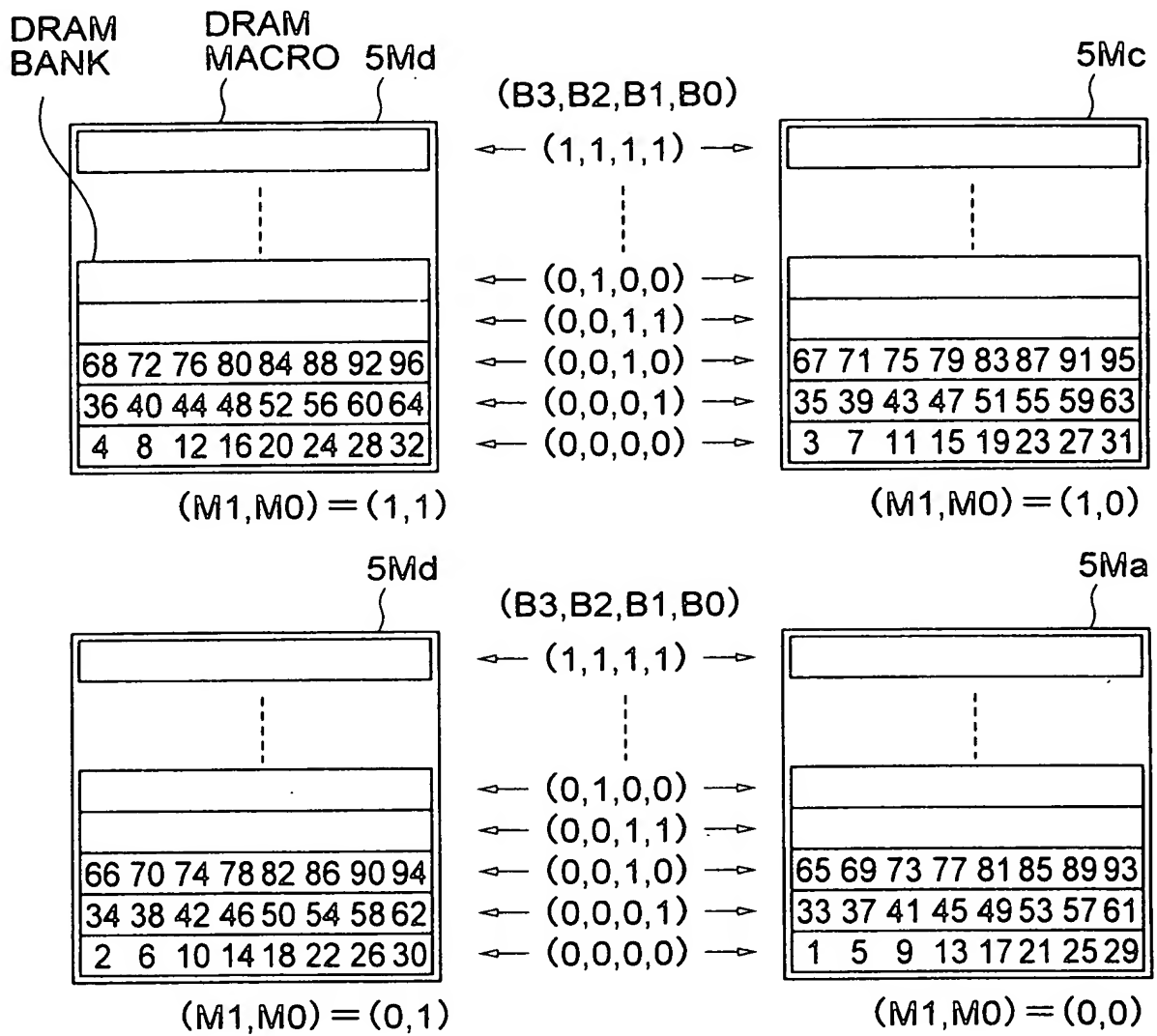


FIG. 15

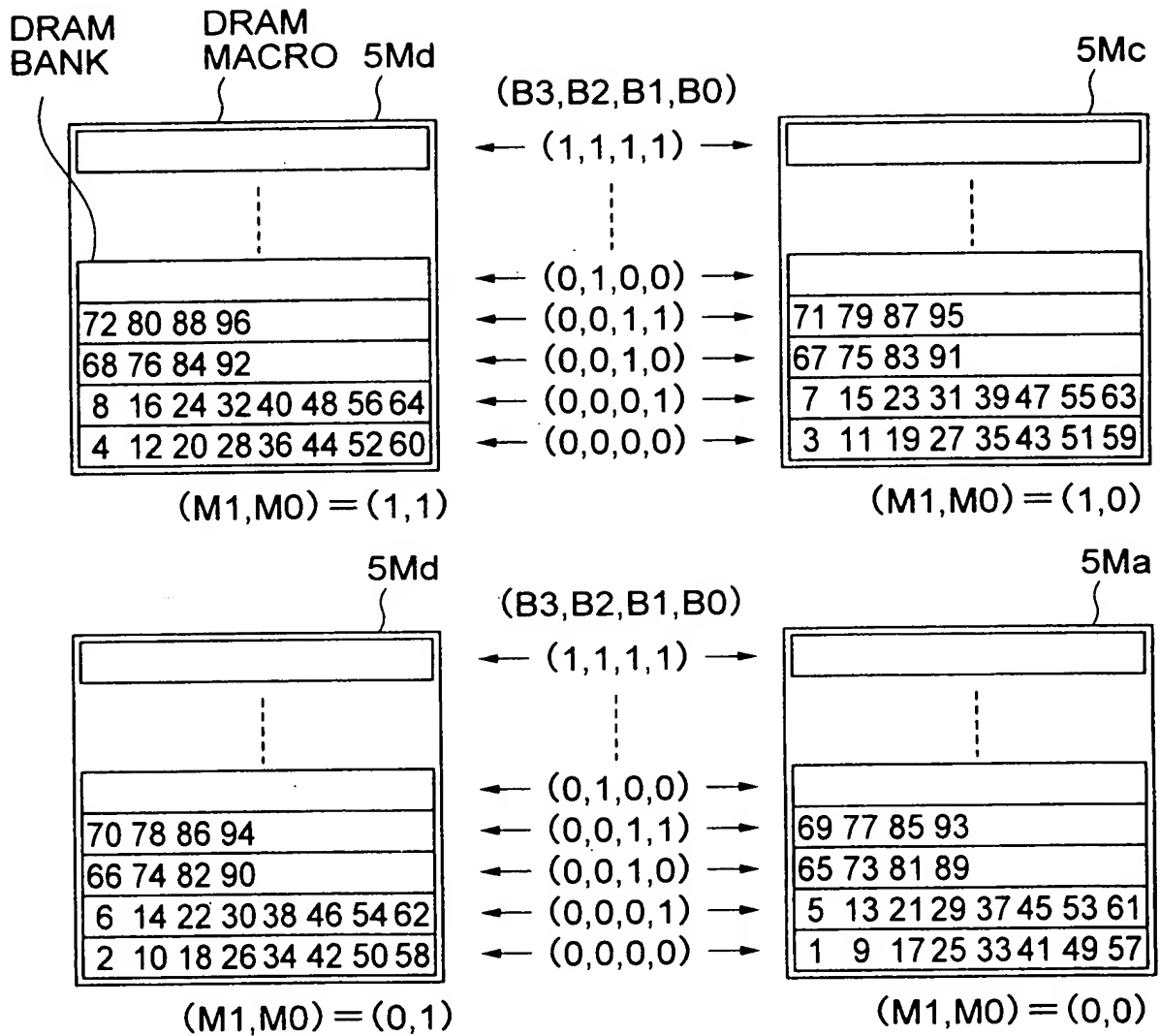


FIG. 16

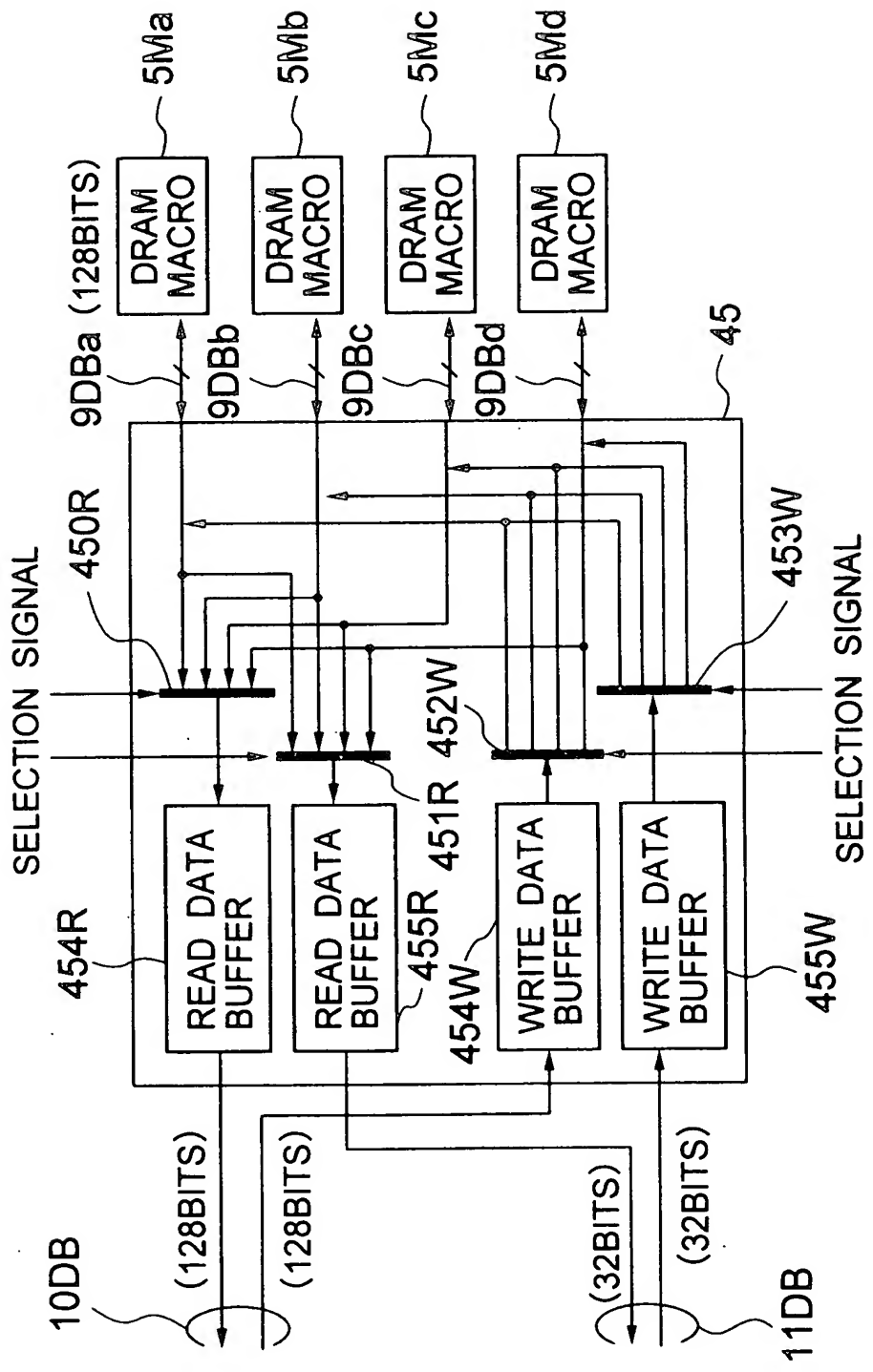


FIG. 17

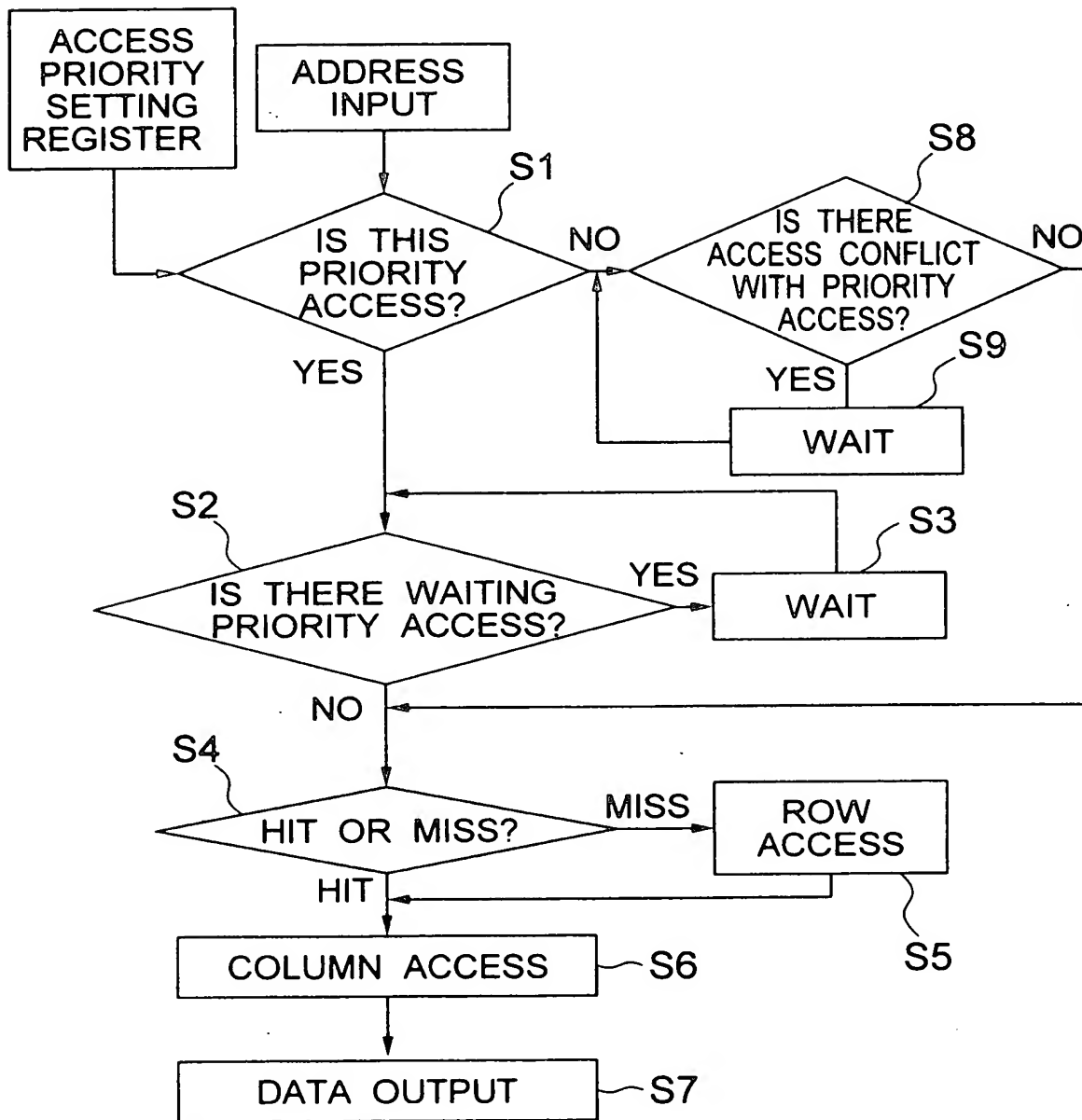


FIG. 18 A

ADDRESS
INPUT aA
(6AB)
ADDRESS
INPUT aB
(11AB)

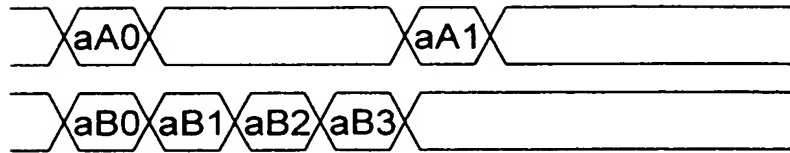
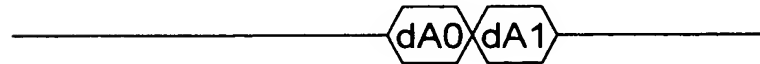


FIG. 18 B

DATA(10DB)



DATA(11DB)

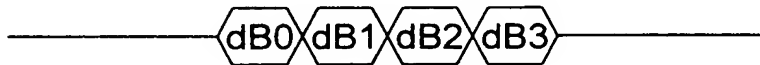


FIG. 18 C

DATA(10DB)

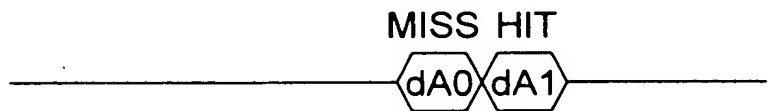


DATA(11DB)



FIG. 18 D

DATA(10DB)



DATA(11DB)

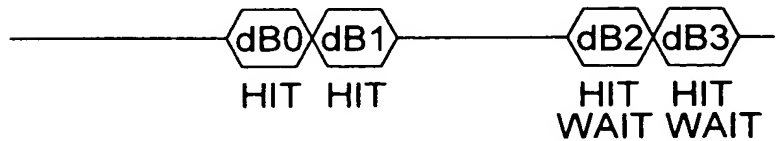


FIG. 19

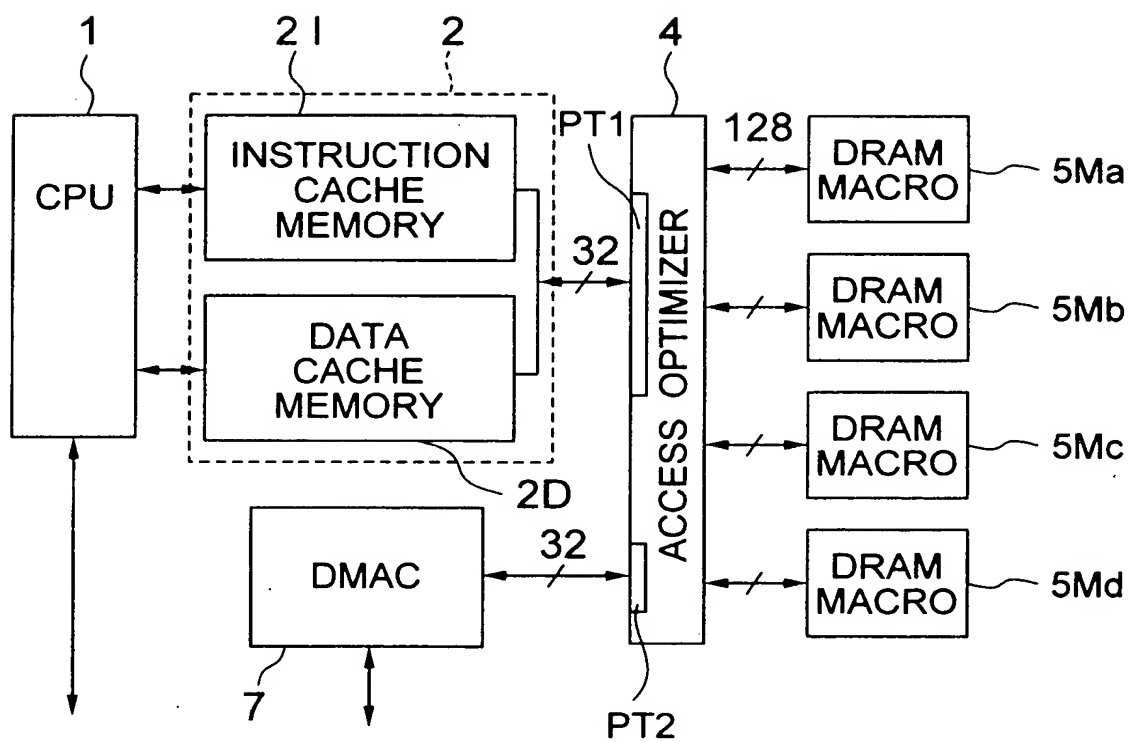


FIG. 20

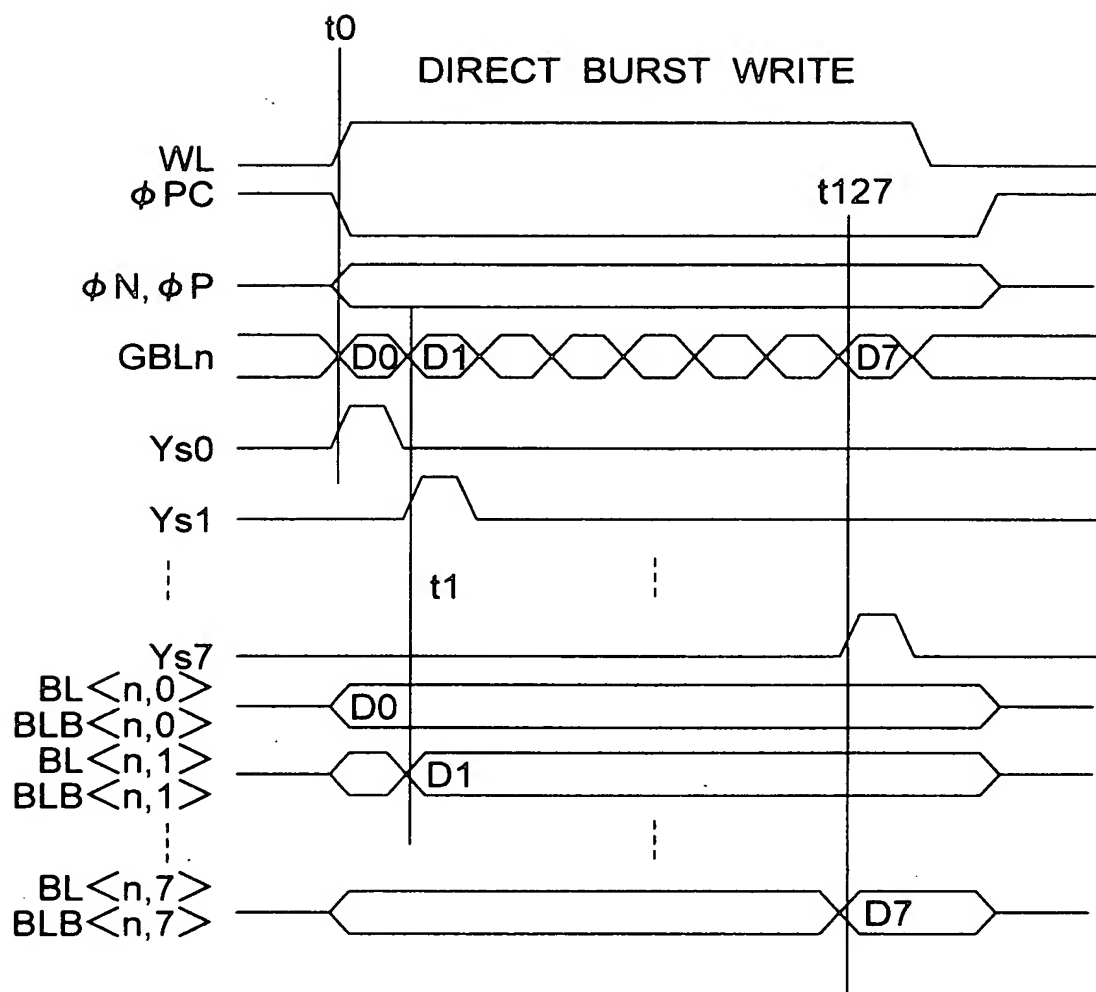


FIG. 21

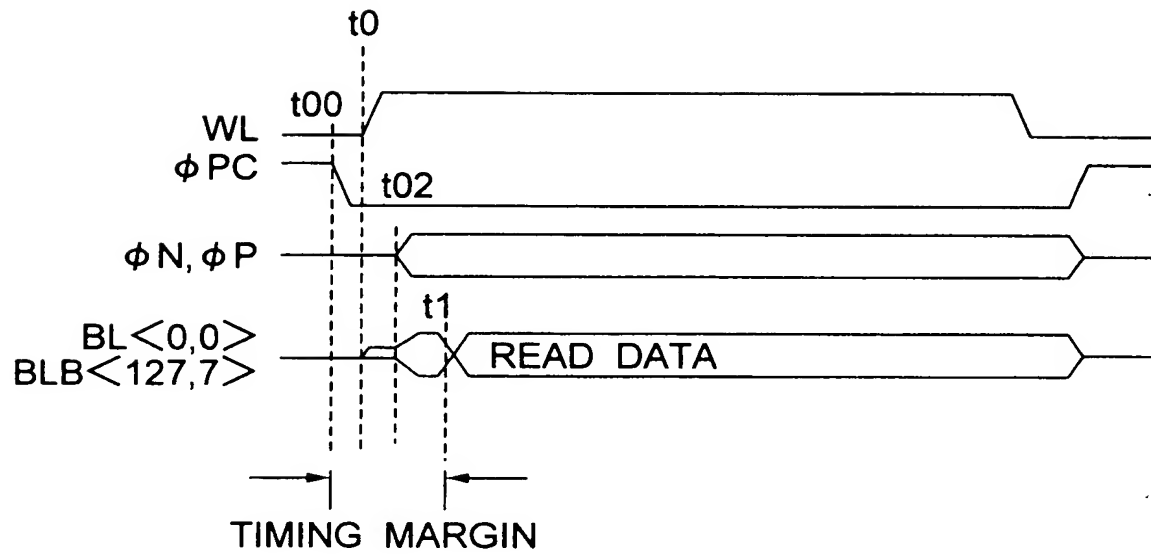


FIG. 22

